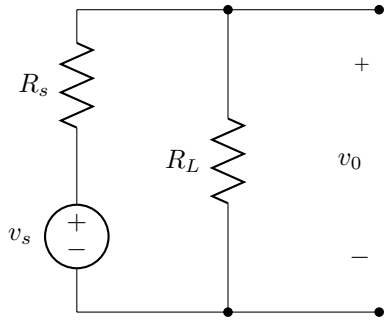
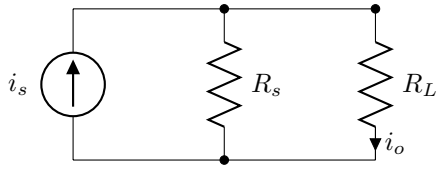
EE113 Book Notes

Lim Soon Wei Daniel

Thevenin Form Voltage source and series resistance.



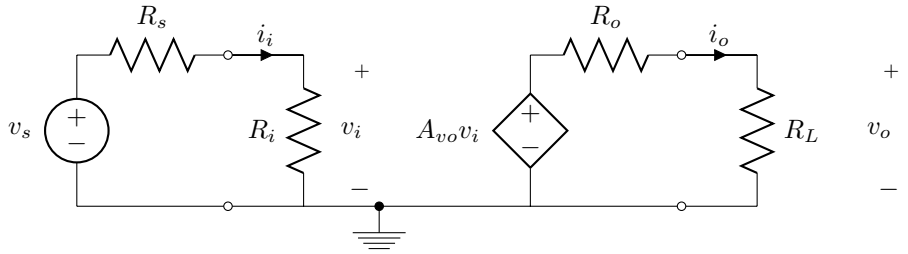
Norton Form Current source and parallel resistance.



Gains $Gain(V) = 20\log|A_v|dB, Gain(I) = 20\log|A_i|dB, Gain(P) = 10\log A_p dB.$

Amplifier power efficiency $\eta = \frac{P_L}{P_{dc}} \times 100$ where P_L is the power delivered to the load and P_{dc} is the power drawn from the DC supplies.

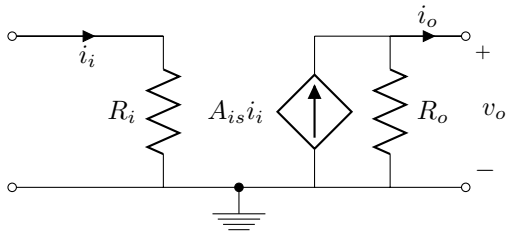
Circuit Model for Voltage Amplifier :



where A_{vo} is the open-circuit gain. Note that the presence of R_s and R_L in the non-ideal case mean that the overall voltage gain is only:

$$\frac{v_o}{v_i} = A_{vo}\frac{R_i}{R_i + R_s}\frac{R_L}{R_L + R_o}$$

Current Amplifier :



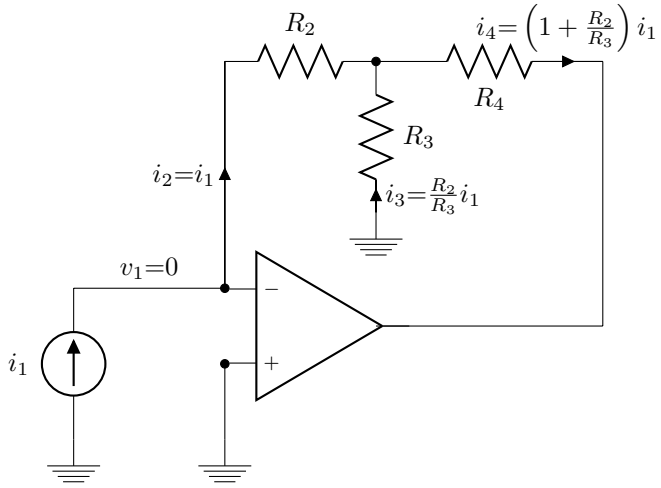
Output Resistance Short all input voltage sources, open all currents. Then place a test voltage at the output port and calculate the ratio of $\frac{V}{I}$ to obtain the output resistance (current in = positive)

Ideal op-amp Infinite input impedance, zero output impedance, zero common-mode gain (=infinite common mode rejection), Infinite open-loop gain A, infinite bandwidth

Finite open loop gain in inverting configuration

$$G = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

Current amplifier Let R_4 be the load (must be floating).



Finite open loop gain in noninverting configuration

$$G = \frac{1 + R_2/R_1}{1 + \frac{1+R_2/R_1}{A}}$$

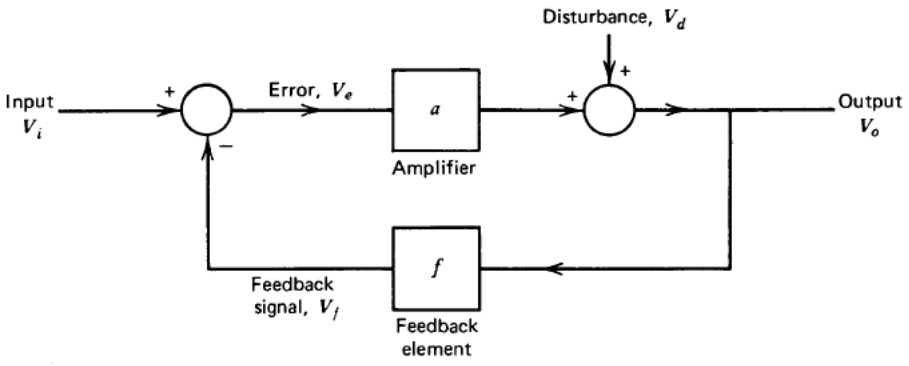
Difference amplifier $v_{Id} = v_+ - v_-, v_{Icm} = \frac{1}{2}(v_+ + v_-)$. $v_o = A_d v_{Id} + A_{cm} v_{Icm}$. Define the Common Mode Rejection Ratio: $CMRR = 20 \log \frac{|A_d|}{|A_{cm}|}$.

Input bias and offset currents

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$
$$I_{OS} = |I_{B1} - I_{B2}|$$

Roberge (1st Edition): Operational Amplifiers: Theory and Practice

Feedback Block Diagram :



with output voltage:

$$V_0 = \frac{aV_i}{1+af} + \frac{V_d}{1+af}$$

Loop transmission For the system above, the loop transmission is $-af$. To find the loop transmission, set all inputs and disturbances to zero, break the block diagram at any point inside the loop, and find the signal returned by the loop (at the point of breaking) in response to a test input signal introduced at the point of breaking.

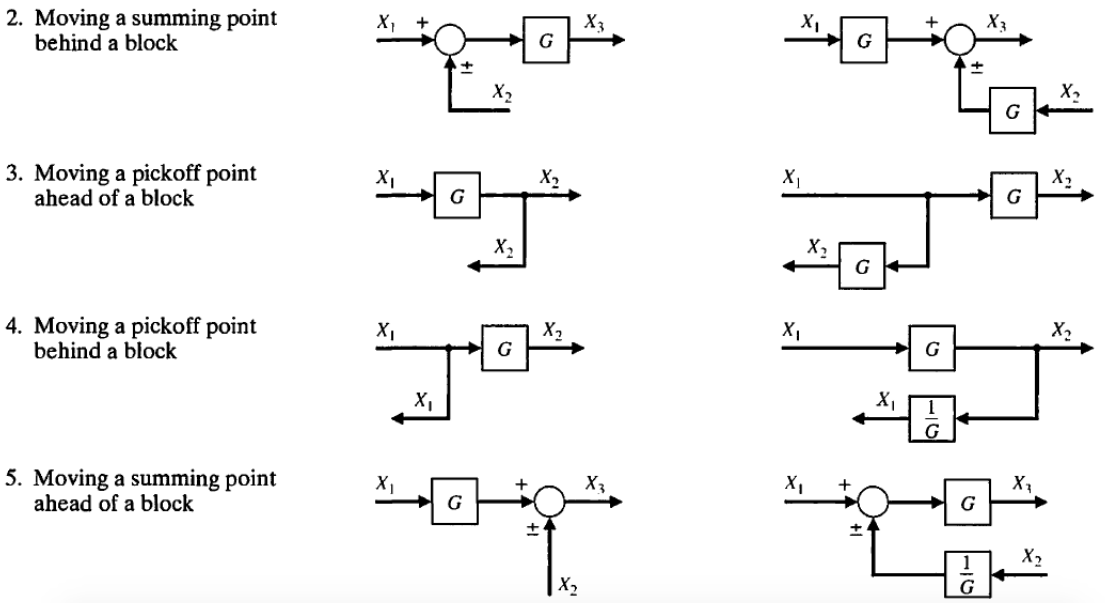
Desensitivity The fractional change in closed-loop gain given by a fractional change in amplifier forward path gain a is:

$$\frac{d(V_o/V_i)}{(V_o/V_i)} = \frac{da}{a}\frac{1}{1+af}$$

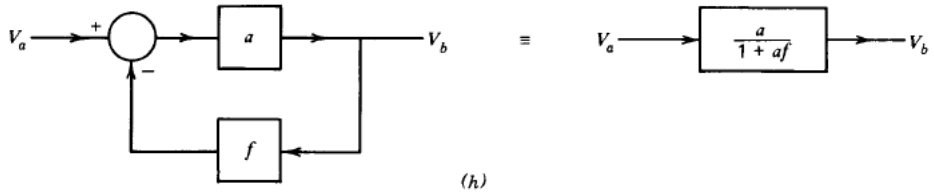
$1+af$ is called the desensitivity, since the larger it is, the less sensitive the gain is to changes in a. It is the ratio of the forward path gain to the closed-loop gain (smaller).

Disturbances The forward-path gain preceding the disturbance results in the relative attenuation of the disturbance.

Block Diagram Simplification from Dorf Pg 81:



Loop reduction :



Gains Path gain: product of all the gains of all elements in a path. Loop: Closed succession of blocks, lines and summation points traversed with the arrows, along which no element is encountered more than once per cycle. Loop gain: product of gains of all elements in a loop.

Closed loop gain

$$T = \frac{\sum_a P_a \left(1 - \sum_b L_b + \sum_{c,d} L_c L_d - \sum_{e,f,g} L_e L_f L_g + \ldots\right)}{1 - \sum_h L_h + \sum_{i,j} L_i L_j - \sum_{k,l,m} L_k L_l L_m + \ldots}$$

P_a is the path gain, so we are summing across all possible paths (must follow forward direction!) connecting the input and the signal of interest. Each path gain is scaled by a cofactor (in brackets), where the second term is all possible loop gains for loops that do not touch the path, the third term is the binary product of all possible loop gains for loops that do not touch the path etc. The denominator is the determinant or characteristic equation of the block diagram, and is equal to 1-loop transmission of the block diagram. Second term in the denominator is all possible loop gains (can touch the path), third term is all possible loop gain products taken two at a time etc.

Impedances under feedback Input and output impedances under feedback can be calculated by taking the impedances without feedback and scaling it up by 1 - loop transmission.

Partial Fraction Decomposition Let $F(s) = \frac{p(s)}{(s+s_1)(s+s_2)\cdots(s+s_n)}$. Then $F(s) = \sum_{k=1}^{n} \frac{A_k}{s+s_k}$ with $A_k = \lim_{s\to -s_k}(s+s_k)F(s)$. For roots with multiplicity, we have terms that look like $\sum_{k=1}^{m} \frac{A_k}{(s+s_i)^k}$, with $A_k = \frac{1}{(m-k)!}\frac{d^{m-k}}{ds^{m-k}}\left[(s+s_i)^m F(s)\right]_{s=-s_i}, k = 1, 2, \ldots, m$.

ILT of repeated root $\mathcal{L}^{-1}\left[\frac{K_n}{(s+a)^n}\right] = \frac{K_n}{(n-1)!}t^{n-1}e^{-at}u(t)$.

Second Independent Variable LT Let $\mathcal{L}[f(t,a)] = F(s,a)$. Then $\mathcal{L}\left[\frac{df(t,a)}{da}\right] = \frac{dF(s,a)}{da}$ and $\mathcal{L}\left[\lim_{a\to a_0} f(t,a)\right] = \lim_{a\to a_0} F(s,a)$.

Final Value Theorem $\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)$ provided no poles of $sF(s)$ are in the right half-plane.

Initial Value Theorem $\lim_{t\to 0^-} f(t) = \lim_{s\to\infty} sF(s)$ provided the limit exists.

Transfer function The ratio of the Laplace transform of the output variable to the Laplace transform of the input variable, with all initial conditions assumed to be zero.

$$\frac{V_o(s)}{V_i(s)} = \frac{a_0 \prod_{i=1}^{m}(\tau_{z,i}s+1)}{\prod_{j=1}^{n}(\tau_{p,j}s+1)}, n > m, \tau > 0$$

$$\implies v_o(t) = \mathcal{L}^{-1}\left[\frac{1}{s}\frac{V_o(s)}{V_i(s)}\right] = a_0 + \sum_{k=1}^{n} A_k e^{-t/\tau_{p,k}} \quad \text{to a unit step input}$$

$$A_k = -a_0 \frac{\prod_{i=1}^{m}(-\frac{\tau_{z,i}}{\tau_{p,k}}+1)}{\prod_{j=1,j\neq k}(-\frac{\tau_{p,j}}{\tau_{p,k}}+1)}$$

Single Pole Approximation If τ_{p1} is much larger than all other τs, then under the unit step input, $A_1 \approx a_0, A_k \approx 0, k \neq 1$. Hence $v_o(t) \approx a_0(1 - e^{-t/\tau_{p,1}})$.

Complex pair Pole Approximation

$$\frac{V_o(s)}{V_i(s)} = \frac{a_0}{s^2/\omega_n^2 + 2\zeta s/\omega_n + 1}$$

ω_n is the natural frequency and ζ is the damping ratio, the ratio of the actual damping to the critical damping. If $\zeta < 1$, the system is underdamped, and so on. ζ is also the cosine of the angle that the complex conjugate roots make with the negative real axis.

Butterworth Filter has poles that are located on a circle entered at the origin.

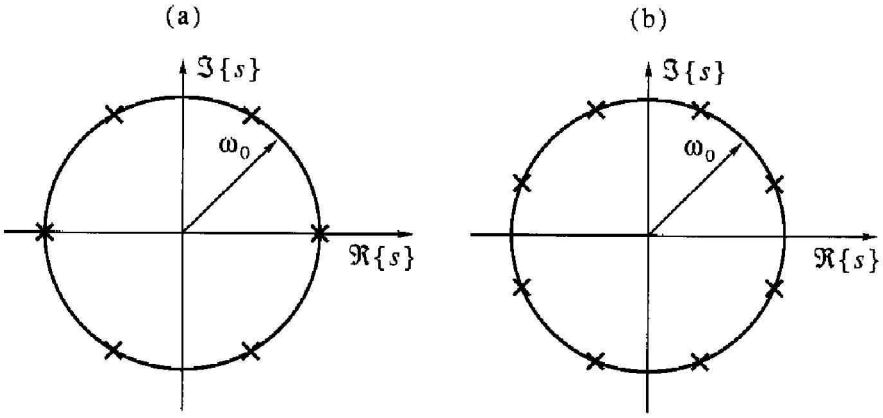
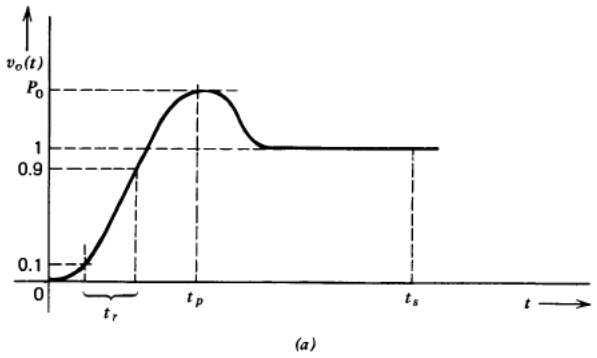


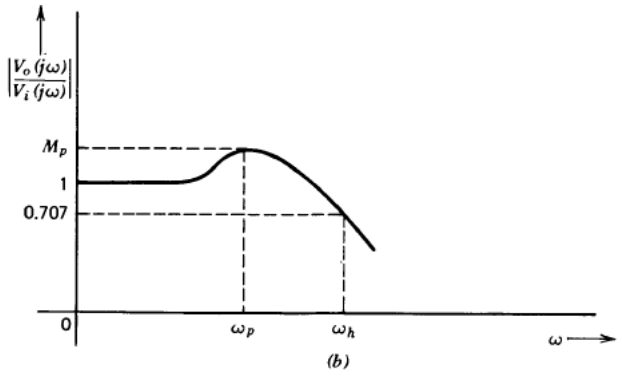
Figure 10.2 The poles of a low-pass Butterworth filter: (a) $N = 3$; (b) $N = 4$. The N poles of $H^{\mathrm{L}}(s)$ are on the left side of the s plane and those of $H^{\mathrm{L}}(-s)$ are on the right side.

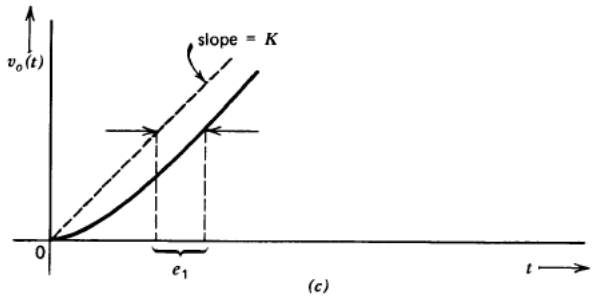
For n even, the poles make angles of $\pm\frac{(2k+1)}{n}90°, k = 0, 1, \ldots, \frac{n}{2} - 1$ with the negative real axis. For n odd, the poles make angles of $\pm k\frac{180°}{n}, k = 1, 2, \ldots, \frac{n-1}{2}$ with the negative real axis.

Parameters :

- Rise time t_r. Time required for the step-response to go from 10% to 90% of the final value.
- Settling time t_s. Time after which the system step response remains within 2% of the final value.
- P_0: maximum value of step-response in time domain.
- t_p: time at which P_0 occurs.
- Error coefficient e_1. Time delay between output and input when the system has reached steady-state conditions with a ramp as its input. Horizontal displacement between the straight lines of the ramp input and the system response at steady state.
- Bandwidth ω_h. Frequency (or angular frequency) at which the response of the system is 0.707 of the low-frequency value.
- M_p maximum magnitude of frequency response
- ω_p, frequency at which M_p occurs.







Notes on Bode Plots In the following, we assume that the pole/zero is in the LH half-plane. If the pole/zero is in the RH half-plane, the magnitude plot remains the same, but the phase plot is negative that of the LH case.

Drawing Bode Plots (Magnitude) :

- Constant coefficient K: Contributes $20\log_{10} K$ constant for all frequencies.
- Zero at origin: s. Rising straight line with gradient 20 dB per decade passing through $\omega = 1$.
- Pole at origin $\frac{1}{s}$. Falling straight line with gradient -20dB per decade passing through $\omega = 1$.
- Zero not at origin $1 + \frac{s}{z}$. Zero contribution up to $\omega = z$, then increase of 20dB per decade.
- Pole not at origin $\frac{1}{1+\frac{s}{p}}$. Zero contribution up to $\omega = p$, then decrease of 20dB per decade.
- Conjugate Poles: $\frac{s^2+2\zeta\omega_n s+\omega_n^2}{\omega_n^2}, \zeta < 1$. Flat zero value until ω_n, then peak there, then $-40dB/$decade onwards.
- Conjugate Zeros: $\frac{s^2+2\zeta\omega_n s+\omega_n^2}{\omega_n^2}, \zeta < 1$. Flat zero value until ω_n, have a valley minimum there, then increase $+40dB/$decade onwards.

Drawing Bode Plots (Phase) :

- Constant coefficient K. If $K > 0$, phase doesn't change. If $K < 0$, $\pm 180°$ shift.
- Zero at origin: Constant $+90°$ shift.
- Pole at origin: Constant $-90°$ shift.
- Zero not at origin: $0°$ up to $0.1z$, $+45°$ per decade increase up to $10z$, then $+90°$ constant onwards.
- Pole not at origin: $0°$ up to $0.1z$, $-45°$ per decade up to $10z$, then $-90°$ onwards.
- Conjugate Poles: Decrease from $0°$ to $-180°$ over $0.1\omega_n$ to $10\omega_n$, achieving $-90°$ at ω_n.
- Conjugate zeros: Increase from $0°$ to $180°$ over $0.1\omega_n$ to $10\omega_n$, achieving $+90°$ at ω_n.

Minimum phase transfer function All poles and zeros are in the left half plane.

Nyquist Stability A minimum phase system should have no encirclements of -1 on the Nyquist plot for stability.

Phase Crossover Frequency Frequency at which the phase of $G(s)H(s)$ is $-180°$. Denoted ω_{PC}.

Gain Margin Reciprocal of the Gain at the phase crossover frequency:

$$GM = \frac{1}{A(\omega_{PC})}$$

For a minimum phase $G(s)H(s)$, the system is stable if $GM > 1$, marginally stable if $GM = 1$ and unstable if $GM < 1$.

Gain crossover Frequency Frequency at which the magnitude of $G(s)H(s)$ is 1. Call this ω_{GC}.

Phase Margin $PM = 180° + \Phi(\omega_{GC})$ where the range of Φ is $[-270°, 90°]$. A minimum phase system is stable if $PM > 0$, marginally stable if $PM = 0$ and unstable if $PM < 0$.

Chapter 1

Week 1

1.1 Thursday 2 Apr 2015

Finding Poles and Zeros We aim to factor the polynomial into 1st and 2nd degree polynomials. The circuit will not work when it contains polynomials of 3rd degree and onwards. As a designer, we can make assumption about the component values, then verify whether the assumptions are still correct later.

Quick factorization Consider the polynomial $1 + a_1 s + a_2 s^2 + \ldots + a_n s^n$. The roots are at $\omega_i = \frac{a_{i-1}}{a_i}, i = 0, 1, \ldots, n$ (actually these are negative values) where $a_0 \equiv 1$.

Important Numbers

$$\log_{10} 2 = 0.30103$$
$$\log_e 3 = 1.09861$$

Maximum error of phase plot (simple pole and simple zero): 5.7° at the intersection of the phase plot lines. Maximum deviation of 5.3° at the middle area.

Effect of right-half-plane zero Same magnitude response, but the phase response is inverted (pole looks like zero and vice versa)

Chapter 2

Week 2

2.1 Tuesday 7 Apr 2015

Office Hours At 014 Moore for now. Lab in 066.

- M 5-6
- W 7-9
- R 4-6, 7-9
- F 4-6, 7-10

Predicting transfer functions We use the phase data to verify what is seen in the magnitude data. Phase is subject to more uncertainty.

Feedback Amplifier Portion of the output is applied to the input. Function is to reduce sensitivity of system to parameter variation.

Cascading Compensation Put a compensation block in front of the amplifier, so the open-loop gain is $G_c(S)G_A(s)$. We may hence shape the gain by choosing $G_c(s)$. But this is still very sensitive to parameter variation.

Feedback Compensation Take the output, apply $H(s)$ as the feedback gain, then subtract this from the input. Then $v_0 = \frac{G_A(s)}{1+G_A(s)H(s)}v_i$. Now pick $G_A(s)H(s) >> 1$. Then the gain is around $\frac{1}{H(s)}$, which is independent of the amplifier gain. $H(s)$ are made of passive components, which can be controlled very well.

Problem with Feedback Compensation: Stability Note that if the loop gain has a 180° phase shift, it is going to result in an increase in the input (because it subtracted). If the gain is greater than unity, then the input will blow up. Then we have issues with stability. To examine stability characteristics, look at $T(s)$.

Measures of stability Gain Margin and Phase Margin. Phase margin is more useful.

Gain margin How far the gain is from 1 (i.e. 0dB) when the phase is 180°. Uses the phase crossover frequency ω_{PC}, which is the frequency when the phase is 180°. Then the gain margin is $-|T(\omega_{PC})|$ (note negative!) For positive gain margin, the gain at the phase cross over frequency is smaller than unity (which is good).

Phase margin How far is the phase from 180° when the gain is 1 (i.e. 0dB). Uses the gain cross over frequency ω_{GC}, the frequency when the gain is 0dB. Then the phase margin is $180° - \Phi(\omega_{GC})$.

Criterion for stability $GM > 0$ and $PM > 0$. Typical PM are around 72° and 60°. GM not so important. Generally, $\omega_{GC} < \omega_{PC}$.

Topics for Quiz 1 KCL/KVL, Root Approximation, Bode Plots

2.2 Thursday 9 Apr 2015

Finding closed loop gain from Bode plots Note that since $A(s) = \frac{1}{H(s)} \frac{T(s)}{1+T(s)}$. When $T(s) >> 1$, then $A(s) \approx \frac{1}{H(s)}$. Then $T(s) << 1$, then $A(s) \approx G(s)$. Connect these domains on the plot.

Improving stability using compensation Two ways: Lower gain so that ω_{GC} is earlier or lower phase so that ω_{PC} is later (for the case where the phase and gain is decreasing).

Gain Compensation Lower gain so that ω_{GC} is sooner and hence PM is larger. Implement by using G_c as a voltage divider. Problem: Decreasing the gain also decreases the loop gain, which decreases the discrepancy factor and hence we do not have good approximation to $\frac{1}{H(s)}$. Hence will have steady-state errors and a much smaller bandwidth. Only use when you need a small amount of adjustment to make. Also changes DC gain.

Dominant pole compensation Introduce a low frequency pole. Doesn't affect DC gain (pole not at origin) (hence no change in steady-state error). But adds $-90°$ of phase shift (hence reduces bandwidth). Hence need to look at the desired phase margin frequency, then set the dominant pole so that the gain is 0dB $90°$ before that frequency.

Op-amps and dominant poles This method is commonly used in op-amp circuits because transistors have lots of high frequency poles and zeroes. Hence we introduce a dominant pole around 1 to 10Hz so that the frequency response curve is nice and easy to work around.

Lag compensation Adjustable pole/zero pair. Want to reduce the gain, but not everywhere. The pole reduces the gain, then the zero (at a higher frequency) cancels out the pole's phase. The α controls the distance between the pole and zero and is governed by how much gain needs to be cut. We need to place the zero 1 decade below ω_{GC}, and the pole is located a distance α before the zero.

Lead Compensation Adjustable zero/pole pair, zero is at lower frequency, separated by α. Objective is to add positive phase to increase the ω_{PC} using a pole. The pole stops the gain increase from the zero. We pick α so that the maximum increase in phase occurs at the gain crossover point of the amount required (thereby controlling PM). Note that $\alpha < 1$ now, so the smaller the α, the wider separation we have. Note that if we use a passive circuit to do the compensation, we will get loss, and hence we are actually doing gain compensation at the same time. Lead compensation keeps the bandwidth high. Design is iterative: Place the peak of the phase increase at the current ω_{GC}. But at that peak frequency, we have gain, which moves the gain crossover to ω'_{GC}. Then move the lead compensation to ω'_{GC} and iterate until we have a consistent position.

Lag-Lead Compensation Perform the lag compensation at low frequencies (drops gain, and far enough away so that the decrease in phase doesn't affect the gain-crossover phase) and lead compensation at high frequencies (increase phase). Two adjustable pole/zero pairs (actually Pole-Zero-Zero-Pole). Requires an iterative design process.

Chapter 3

Week 3

3.1 Tuesday 14 April 2015

Second order pole, step response Overdamped = Slowly approach from below, Underdamped = Exponentially decaying oscillation. Critically damped = one overshoot, then approach from above - fastest response without oscillation.

Passive Circuit cannot create gain above 0dB? How about transformers

Checking Answers :

- Solve the problem again using a different technique
- Plug numerical values back into the original problem (roots should give zero etc)
- Dimensional analysis
- Sanity checks - check extreme conditions

Op-amps Types: BJT, MOSFET/JFET, BiFET (BJT and FET)

Non-infinite open circuit gain Consider $A(s) = \frac{G(s)}{1+G(s)H(s)}$. Then the larger the required gain, the smaller the $H(s)$ and hence the larger the error.

3.2 16 Apr 2015 Thursday

Op-amp design The biggest non-ideal effect is $K \neq \infty$. If $Z_i \neq \infty$, we want to choose resistances such that $R << KZ_i$. If $Z_0 \neq 0$, then we want to choose $R >> \frac{Z_0}{K}$. Since the smallest K we will work with is 10, we will implement a weaker condition on the resistances:

$$R < Z_i$$
$$R > Z_0$$

Low values of Z_i are around $2M\Omega$. Typical values high of Z_0 are around 100Ω.

Note further that op-amps typically have maximum output currents in the range of milliamps. Hence we have the general guideline:

Keep op-amp resistances in the kilo-ohms! Better on order of 10k or 100k

Lab stuff In 066 Moore, combination 3-45-1

Narrow-band Voltmeter Measurement of the voltage level in a very narrow range of a specific frequency.

Chapter 4

Week 4

4.1 Tuesday 21 Apr 2015

Evaluating block gains in Augmented Feedback Model

$$H_\infty = \left.\frac{1}{A}\right|_{G=\infty}$$
$$H_0 = A|_{G=0}$$
$$G = \left.\frac{v_0}{v_i}\right|_{v_0=0} \quad \text{Gain without feedback}$$

Additional Op-Amp Non-idealities :

- **Gain-Bandwidth Product** (GBW): Recall that op-amps were compensated using a dominant pole. On the dominant pole slope, $f \times K$ is a constant. This is the gain-bandwidth product. Suppose there is an op-amp with a Gain-Bandwidth product of 1MHz. Then the gain at $100kHz$ is 10. The op-amp dominant pole is around 1Hz-100Hz. This GBW gives you the range of frequencies you can use so that the gain is large.
- **Input offset voltage**: When $v_+ = v_-$, the output is non-zero. The input offset voltage is defined to be $v_+ - v_-|_{v_0=0}$, the difference between the inputs such that the output is zero. Usually millivolts.
- **Input bias current**: The current needed to bias the BJT or the leakage current for the FET. This can be removed in the inverting amplifier by placing a resistor at the positive input with value equal to $R_1 \parallel R_2$ so that the currents flowing through the inputs do not result in a voltage difference across the inputs that will lead to a voltage error. Generally, we want to match the impedances on the inverting and non-inverting inputs. If we do so, then we only need to worry about I_{OS}.
- **Input Offset Current** is defined to be $I_{OS} = I_{bias,+} - I_{bias,-}$. The offset current can usually be made smaller than the individual bias currents.
- **Common Mode Rejection Ratio** (CMRR) is defined to be:

  $$\left.\frac{v_0}{v_+ - v_-}\right|_{v_+=v_-=A\cos(\omega t)}$$

  Ideally, we should see no output because the inputs are in sync. But we do see a sine wave output. This has value of around -90dB.
- **Power Supply Rejection Ratio** (PSRR) measures how much power supply noise gets into v_0. Typically in the -90dB range.

Comparison of Op-amps

Parameter	$LM741$	$LM324$	$TL074$
Z_{in}	$1M\Omega - 6M\Omega$	–	$10^{12}\Omega$
GBW	$430kHz - 1.5MHz$	$1MHz$	$3MHz$
V_{OS}	$4mV$	$9mV$	$13mV$
I_{BIAS}	$210nA$(BJT)	$500nA$(BJT)	$7nA$(FET)
I_{OS}	$70nA$	$150nA$	$10nA$

Two-Port Networks Any circuit can be characterized using 2-ports. But usually gives high entropy expressions. The four constants can be understood as follows:

- X_{11} The Port 1 admittance/impedance with Port 2 open/shorted
- X_{22} The Port 2 admittance/impedance with Port 1 open/shorted.
- X_{21} similar to the forward transmission.
- X_{12} similar to the internal feedback.

4.2 Thursday 23 Apr 2015

Chapter 5

Week 5

5.1 Tuesday 28 Apr 2015

Large Signal vs Small Signal Analysis Use small signal analysis to be able to use linear approximations. Notation: use capital letters for large signals, use lowercase for small signals, for combined signals use a mixture of uppercase and lowercase letters.

Transistors Two main types: BJTs and FETs. Think of BJTs as current amplifiers and FETs as a voltage-controlled resistor (transimpedance amplifier).

	BJT	FET
Z_{in}	Low	High
Gain	Higher	Lower
High frequency	Better	Slightly worse
Distortion (Linearity)	Worse	Better

BTJ Current Amplification Factor β, around $20 - 500+$. Is a function of base width and minority carrier lifetime in the base, which are process and temperature dependent (for the minority carriers). Also depends on the operating point. In other words, β is not well defined.

5.2 Thursday 30 Apr 2015

BJT amplifiers BJT is a three terminal device. When we examine it as a two port network, one of the three terminals will be common between the input and output. This gives three different amplifier configurations:

- Common Emitter (CE)
- Common Collector (CC)
- Common Base (CB)

Biasing Transistors i.e. setting the operating point (quiescent point) to determine the possible output voltage swings. For a cascaded amplifier, the voltage swing only really matters for final 2 stages. Last stage is a buffer stage with no gain. Second last stage is the last voltage gain stage.

Biasing also determines the power dissipation.

Steps to perform biasing for a Common-Emitter Amplifier

1. Find Load Line:

   Recall that we want to set I_C and V_{CE}. The load line gives all the possible values for I_C and V_{CE}. This is determined by the load on the transistor circuit itself.

   There are two different load lines: the DC and AC. Use the DC load line to set the bias. The AC load line is what we operate on.

   DC load line: Plot I_C against V_{CE}. It will be a straight line. Pick a quiescent point Q on the DC load line. Choose this point based on the voltage swing. E.g. to get maximum voltage swing, pick it somewhere in the middle.

   Also ensure that you don't go over the maximum power dissipation P_D. Draw the curve $I_C V_{CE} = P_D$. We want to pick a point Q under this curve.

   To find the AC load line, short the power supply. This plot of I_C against V_{CE} will be steeper than the DC load line. When the circuit oscillates, the circuit moves along the AC load line, but it has to pass through the quiescent point along the DC load line. Note that because the AC load line is steeper, it reduces the positive voltage swing in V_{CE}. This has the effect of moving the Q point to the right. Hence, to maximize the voltage swing, we like to pick a point to the left of the center on the DC load line.

   We also have to avoid the linear saturation region.
   The net effect of this step gives I_C (and bias current I_B) and V_{CE}.

2. Find Bias Current

$$I_C = \beta I_B \implies I_B = \frac{I_C}{\beta}$$

   But we need to determine what value of β to use. Use the typical value (or midpoint) as supplied in the datasheet.

3. Design Bias Network

   Three options: Single Bias resistor, Bias divider network and Current Source.

4. Stabilise bias point through feedback

   We face the problem that the actual value of β has quite a bit of variance. We want to stabilise the bias point (note that the bias point is associated with the DC response) so that it does not depend a lot on β. There are two techniques:

   - V_{CB} feedback: Feedback from the collector to the base. Suppose the value of β is actually larger than expected. Then I_C increases, which forces v_o to a lower potential. Then the current that feeds I_B deceases, which indicates that we have negative feedback. The opposite happens if β is actually lower than expected.
   - Emitter degeneration: Sample I_E and feedback into V_B. Increase in β increases the potential of the emitter, which increases the potential of the base, which increases the current through R_{b2} and decreases the current through R_{b1}. These have the effect of decreasing I_B, as anticipated of negative feedback.

Chapter 6

Week 6

6.1 5 May 2015

Comparison of biasing methods Bias Network method is more sensitive to transistor-to-transistor variations because of its stronger dependence on V_{BE}, which also varies based on individual transistors.

Effect of temperature Hitting the transistor circuit with the freeze spray has the effect of changing β. Putting in feedback reduces the magnitude of these fluctuations. Lower temperature seems to reduce β.

Tradeoff Note that the more feedback you put in (such as through increasing R_E) in emitter degeneration, you decrease the voltage swing and decrease AC gain. This can be mitigated by putting a big capacitor in parallel with R_E, which is an AC short and DC open.

Note about bandwidth The bandwidth should be measured with the closed loop response, and is the frequency such that the closed loop gain is half that of the DC gain.

Note about phase margins Critical damping $\delta = 0.707$ corresponds to around 72° of phase margin.

Avoiding Algebra Consider $\frac{1}{R_1}(R_1 \parallel R_L \parallel \frac{1}{sC_2} \parallel (R_2 + \frac{1}{sC_1}))$. Observe that the DC gain is just $\frac{R_1 \| R_L}{R_1}$. As the frequency increases from zero, we note that the smaller of $\frac{1}{C_1}$ and $\frac{1}{C_2}$ will begin to come into play first. If R_2 is small compared to $R_1 \parallel R_L$, there will be a pole at $\frac{1}{C_1(R_1 \| R_L)}$.

Chapter 7

Week 7

7.1 Tuesday 12 May 2015

Definition of input and output impedance

$$Z_{in} = \left.\frac{V_{in}}{I_{in}}\right|_{I_{out}=0}$$
$$Z_{out} = \left.\frac{V_{out}}{I_{out}}\right|_{V_{in}=0}$$

Multi-stage amplifier design Effectively, we want to combine individual gain stages. However, we have loading on each stage, and we are also picking up lots of poles and zeros. To avoid noise problems, we want to introduce gain as soon as possible. For a voltage amplifier, we want a high input impedance. Hence we pick a common emitter first stage as a compromise between high input impedance and high gain for the first stage. Alternatively, use a differential amplifier for the first stage (useful because you can send the feedback into one of the ports).

For the output stage, we want a common collector stage because of the low output impedance.

Stage coupling: Can be either AC or DC. For AC coupling, just connect with a big capacitor between stages. This is useful to ensure that the bias points of each stage are independent of each other. However this adds lots of low frequency poles. The pole position is approximately equal to $\frac{1}{C(Z_{out}+Z_{in})}$ at the position of the capacitor. We need to separate these low frequency poles otherwise we will get low frequency oscillations.

DC coupling: Quiescent output of stage i is the bias point of stage $i+1$. The bias points keep increasing in voltage, hence it is easy to run out of headroom. The solution if you are biasing with voltages is to include a stage with a complementary transistor (PNP if we are using NPN transistors) to bias in the opposite direction. If you are biasing with currents, there are no issues. Hence we want to create current sources to bias the transistors (at the emitter).

7.2 14 May 2015

Multistage Amplifier Design :

- Input stage: Typically Common Emitter (gives gain and high input impedance) or a Differential Amplifier

- Middle Stages: Gain Stages and Special Purpose Stages
- Final Stage: Typically Common Collector (Buffer stage)
- Feedback (into Input Stage)

Interstage Loading Each stage is located by the following blocks (depending on the input impedance of the following block). But we had that for each of the CC, CE, CB configurations, the input impedance was a function of the load that stage experiences. **Hence we need to compute the loading from right (output) to left (input) to calculate the input impedance. Proceed from the left to right to calculate the output impedance.** The input impedance of a stage is the load impedance of the previous stage.

Feedback We can improve the overall gain and characteristics by improving the input and output impedances. However, there may be Transient Intermodulation Distortion (TIM) for large feedback because there is a finite time taken for the signal to return to the input.

Stability Each stage has poles and zeros. To fix this, make one stage dominant using Biasing.

AC coupling gives inverted poles (zero at origin and normal pole). To fix the AC coupling issue, make one of the poles dominant (first pole to be encountered when coming down from midband).

If the loop gain $T(s)$ is very large we can use dominant pole compensation to avoid stability issues.

Control Systems Types of control: Classical Control and Modern Control. Classical Control uses Nyquist and Bode Plots, works in the frequency domain and uses compensation. This works for many systems. But this does not work for multi-input and multi-output systems.

Modern control deals with multi-input-multi-output (MIMO) systems. It started off by using state space.

Comparison between Feedback Amplifiers and Control Systems For both, stability is very important. For Feedback Amplifiers, Input/Output Impedance is important. But in the control system, Input/Output impedance is not important. For feedback amplifiers, disturbances are not important. But for control systems, disturbances are important. In feedback amplifiers, we need to design the whole system. In a control system, you only can design the controller. In that way, we have a lot of control over parameters in a feedback amplifier but very little in the Control system.

- Can use 1N5226?
- Need to buffer base driving voltage? How do deal with open loop overshoot?
- Calculation of open-loop parameters.
- How to choose N in the practical D compensation?
- Unable to see the entire step response, only the AC coupled version - even with 10x probes. How to measure rise time?
- We only take the derivative of the feedback so that it is not sensitive to changes in the reference point.

Chapter 8

Week 8

8.1 19 May 2015

Quiz Topics Transistors + Transistor Circuits, Biasing, Circuit configurations, models for transistor.

P compensation Suppose $G(s) = \frac{a_0}{s^2+c_1 s+c_0}$, $H(s) = 1$. Then:

$$A(s) = \frac{K_p G(s)}{1 + K_p G(s) H(s)} = \frac{K_p a_0}{s^2 + c_1 s + c_0 + K_p a_0}$$

where we have proportional cascade compensation at the $G(s)$ block. Note that:

$$\omega_n = \sqrt{c_0 + K_p a_0}$$
$$\delta = \frac{c_1}{2\sqrt{c_0 + K_p a_0}}$$

hence increasing K_p will increases the ringing frequency (more ringing) and decrease δ, which gives more overshoot.

Ziegler-Nichols' Use quarter decay criteria: 2nd overshoot is 25% of 1st overshoot.

8.2 Thursday 21 May 2015

Final Value Theorem

$$\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)$$

The error term is:

$$E(s) = \frac{R(s)}{1 + G(s)H(s)}$$

where $R(s)$ indicates the type of input:

$$R(s) = \begin{cases} \frac{1}{s}, & \text{Unit step} \\ \frac{1}{s^2} & \text{Unit ramp} \\ \frac{1}{s^3} & \text{Unit Parabola} \end{cases}$$

System Order/Type is the number of integrators in the loop gain GH.

Routh-Hurwith Tells you how many RHP poles there are.

Root Locus Plot Tells you how the roots move as you change the gain.

Root Locus Example Consider $G = \frac{K}{s(s+\beta)}$. Then the closed loop gain is:

$$A = \frac{G}{1+GH} = \frac{K}{s^2+\beta s+k}, \quad H = 1$$

Hence the parameters are:

$$\omega_n = \sqrt{k}$$
$$\delta = \frac{\beta}{2\sqrt{k}}$$

Nyquist plots A polar plot of response as a function of frequency.

Cauchy's Theorem If P = number of poles and Z = number of zeros of some function $F(s)$ that are enclosed by a closed clockwise contour Γ_s in the s-plane, then the net number of times Γ_F in the F-plane encircles the origin is $N = P - Z$ in the clockwise direction.

Chapter 9

Week 9

9.1 Tuesday 26 May 2015

Breadboard configuration Note that there is about $5pf$ of capacitance between adjacent rows. To enhance the cascode high frequency response, shift the base and collector to rows in different columns.

Servo motor control Use pulse width modulation. Astable multivibrator sends trigger pulses into a monostable multivibrator. The latter controls the pulse width. By changing the input voltage you change the reference voltage to the monostable circuit.

Limitations of Classical Control Limited to Single Input Single Output systems (SISO) and Time-Invariant systems.

State-Space Control